

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

1 **Claim 5 (currently amended):** A semiconductor device,
2 comprising:

3 ~~which is formed by~~ combining and disposing means for
4 combining and disposing pre-registered functional blocks,
5 and

6 wiring means for determining a wiring pattern in
7 accordance with a given logic circuit specification,
8 ~~wherein:~~

9 wherein at least one of the functional blocks has a
10 logic circuit and a diode, ~~and~~

11 the diode is composed of a first conduction type
12 diffusion layer and a second conduction type well connected
13 to a power source, and

14 the diode is connected to a potential-clamped input
15 terminal of the at least one of the functional blocks.

1 **Claim 6 (previously presented):** The semiconductor
2 device as claimed in Claim 5, wherein the logic circuit is
3 a memory.

1 **Claim 7 (currently amended):** A method of designing a
2 semiconductor device, comprising the steps of:
3 ~~which is formed by~~ combining and disposing pre-
4 registered functional blocks, and
5 determining a wiring pattern in accordance with a
6 given logic circuit specification, ~~comprising the steps of:~~
7 ~~registering the functional blocks in advance,~~
8 wherein at least one of the functional blocks has a
9 logic circuit and a diode, ~~and~~
10 ~~wherein~~ the diode is composed of a first conduction
11 type diffusion layer and a second conduction type well
12 connected to a power source, and
13 the diode is connected to a potential-clamped input
14 terminal of the at least one of the functional blocks.

1 **Claim 8 (previously presented):** A computer-readable
2 recording medium, on which the method of designing a
3 semiconductor device, as claimed in Claim 7, is stored as
4 a program to be executed by a computer.

1 **Claim 9 (currently amended):** A design support
2 apparatus for a semiconductor device, comprising:
3 ~~which is formed by~~ combining and disposing means for
4 combining and disposing pre-registered functional blocks,
5 and
6 wiring means for determining a wiring pattern in

7 accordance with a given logic circuit specification,
8 ~~comprising:~~

9 ~~registration means for registering the functional~~
10 ~~blocks in advance,~~

11 wherein at least one of the functional blocks has a
12 logic circuit and a diode, and

13 wherein the diode is composed of a first conduction
14 type diffusion layer and a second conduction type well
15 connected to a potential-clamped input terminal of the at
16 least one of the functional blocks.

1 **Claim 10 (currently amended):** A semiconductor device,
2 comprising:

3 ~~which is formed by combining~~ combining and disposing
4 means for combining and disposing pre-registered functional
5 blocks, and

6 wiring means for determining a wiring pattern in
7 accordance with a given logic circuit specification,
8 ~~wherein:~~

9 wherein at least one of the functional blocks
10 ~~including functional blocks~~ has a logic circuit and a diode
11 which is at least connected to an input pin where results
12 of an antenna ratio exceed an allowed antenna ratio, ~~and~~
13 the diode is composed of a first conduction type
14 diffusion layer and a second conduction type well connected
15 to a power source, and

16 the diode is connected to a potential-clamped input
17 terminal of the at least one of the functional blocks.

1 **Claim 11 (previously presented):** The semiconductor
2 device as claimed in Claim 10, wherein the logic circuit is
3 a memory.

1 **Claim 12 (currently amended):** A method of designing a
2 semiconductor device, comprising the steps of:
3 ~~which is formed by~~ combining and disposing pre-
4 registered functional blocks, and
5 determining a wiring pattern in accordance with a
6 given logic circuit specification, ~~comprising the steps of:~~
7 ~~registering the functional blocks in advance,~~
8 wherein at least one of the functional blocks has a
9 logic circuit and a diode which is at least connected to an
10 input pin where results of an antenna ratio exceed an
11 allowed antenna ~~ration,~~ ratio,
12 wherein the diode is composed of a first conduction
13 type diffusion ~~later~~ layer and a second conduction type
14 well connected to a power source, and
15 the diode is connected to a potential-clamped input
16 terminal of the at least one of the functional blocks.

1 **Claim 13 (previously presented):** A computer-readable
2 recording medium, on which the method of designing a

3 semiconductor device, as claimed in Claim 12, is stored as
4 a program to be executed by a computer.

1 **Claim 14 (currently amended):** A design support
2 apparatus for a semiconductor device, ~~comprising:~~

3 ~~which is formed by~~ combining and disposing means for
4 combining and disposing pre-registered functional blocks,
5 and

6 wiring means for determining a wiring pattern in
7 accordance with a given logic circuit specification,
8 ~~comprising:~~

9 ~~registration means for registering the functional~~
10 ~~blocks in advance,~~

11 wherein at least one of the functional blocks has a
12 logic circuit and a diode which is at least connected to an
13 input pin where results of an antenna ratio exceed an
14 allowed antenna ratio, and

15 wherein the diode is composed of a first conduction
16 type diffusion layer and a second conduction type well
17 connected to a potential-clamped input terminal of the at
18 least one of the functional blocks.

1 **Claim 15 (new):** The semiconductor device as claimed in
2 Claim 5, wherein the diode is connected to a port between
3 an output of the logic circuit and the input terminal of
4 the functional block.